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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/726,342

12/03/2003

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15098US01

9025

23446 7590 06/07/2010  
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EXAMINER

CAMPOS, YAIMA

ART UNIT

PAPER NUMBER

2185

MAIL DATE

DELIVERY MODE

06/07/2010

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/726,342	<b>Applicant(s)</b> ANAND, ANUPAM	
	<b>Examiner</b> YAIMA CAMPOS	<b>Art Unit</b> 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 05 March 2010.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-10, 12-15, 24, and 26-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                    | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)         | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. As per the instant Application having Application number 10/726,342, the examiner acknowledges the applicant's submission of the amendment dated 3/5/2010. At this point, claims 10-13, 15, 24 and 26 have been amended and claims 11, 16-23, 25 and 28-40 have been cancelled. Claims 1-10, 12-15, 24 and 26-27 are pending.

### **REJECTIONS NOT BASED ON PRIOR ART**

#### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-9 and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. As per claims 1 and 24, Applicant's Specification does not contain support for the limitations of "wherein the first state comprises at least a portion of a memory address of the first memory block, irrespective of a position of the first logic circuit" (claim 1) and "wherein the first state comprises at least a portion of a memory address of the block of memory segments irrespective of a position of the first logic circuit" (claim 24) since in Applicant's Specification, the addresses of memory blocks are related to the position of the identified available blocks

Art Unit: 2185

within logic circuits indicating block availability. For example, **(refer to figs. 2-9 and related text)** which illustrate addresses of identified available memory blocks corresponding to the position of logic circuits 450. Further, the recitation "For example, various information may be contained in the segment or block flags that the step 1040 may utilize to calculate the segment address. Alternatively, for example, the step 1040 may convert the position of the identified segment flag in the set of segment flags to the address of the memory segment" (Specification, page 27, paragraph 90) does not teach the flag comprising a portion of the memory address of an available segment, irrespective of a position of the first logic circuit. The Specification only vaguely recites "various information may be contained in the segment or block flags that the step 1040 may utilize to calculate the segment address"; without specifying anywhere what kind of information may be contained in the segment or block flags or whether addresses of segments or blocks are "irrespective of the position of the first logic circuit" or the logic circuit comprising information indicating memory availability.

5. Any claims not addressed above are rejected because they depend on a rejected base claim.

## **REJECTIONS BASED ON PRIOR ART**

### **Claim Rejections - 35 USC § 103**

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 2185

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 1-9 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldberg (US 6,874,062) in view of Lehman (US 6,658,437) and further in view of Rozario et al. (US 2004/0078525).

8. As per **claim 1**, Goldberg discloses A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising: **[Goldberg discloses “an Operating System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System” (Col. 7, lines 11-13) wherein “Files can further be subdivided into smaller addressable portions of memory called “sections,” (interpreted to correspond to the claimed memory segments) wherein each section has a same predetermined size” (Col. 7, lines 22-26) and explains grouping sections into segments (interpreted to correspond to the claimed memory blocks) (Col. 8, lines 49-65) (Figures 1 and 2 and related text)]** a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage **[Goldberg discloses bitmap 1 (interpreted to correspond to the claimed first logic circuit) wherein “in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File” (Col. 8, lines 43-48) and explains “the LLB may be divided into**

Art Unit: 2185

**Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to “0” if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to “1” if all bits in the corresponding LLB Segment are set” (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein “a bit is set if a Section is in use and is cleared if the Section is available for allocation” (Col. 7, lines 50-61)]**

wherein the first state includes at least a portion of a memory address of the first memory block [Goldberg discloses “in step 814 processing is completed and the memory address associated with the located available memory sections may be returned to the requested” (Col. 12, line 26-29) and discloses “a data structure that may be used to store the Hierarchical Bitmap Structure of the current invention... a level descriptor for each of the individual bitmaps in the Bitmap Packet 1002. This level descriptor includes information such as the starting address and bit-length of the corresponding bitmap” (Col. 15, lines 19-40; Figure 10 and related text)].

Goldberd does not explicitly disclose the details of having the first state include at least a portion of a memory address of the first memory block, irrespective of a position of the first logic circuit.

Art Unit: 2185

Lehman discloses having the first state includes at least a portion of a memory address of the first memory block as [**“The DBMS 24 receives database requests from the clients 28 and performs data access operations to storage and retrieve referenced data values from the storage subsystem 30... the DBMS 24 maintains data structures called allocation pages that keep track of data storage availability” (Col. 3, line 61-Col. 4, line 37) having an allocation array wherein “blocks larger than 1 can start only on an appropriate block address... the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two” (Col. 11, lines 38-46) (Figure 7 and related text) and explains “the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array... For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks” (Col. 10, line 50-Col. 11, line 15) (Figure 9 and related text) and explains “FIG. 9 shows an allocation array that includes 5 groups of bitmaps each having 16 bits... there are 16 bits in a group, each having 16 address locations numbered 0-15” (col. 10, lines 50-60)]; therefore, bits which represent a first state and indicate availability of a memory block correspond to bits having “a first state” wherein since the bit position of these bits has a memory address, thus, disclosing first state includes at least a portion of a memory address of the memory block having available memory, as claimed. Note that the bits representing a first state in Lehman have a direct**

Art Unit: 2185

**correspondence with their calculated memory address, thereby, “*comprising*” at least a portion of their memory address].**

Rozario discloses a logic circuit having a state indicating availability of memory, wherein a state indicating memory availability comprises at least a portion of a memory address, irrespective of a position of the first logic circuit as [**“each memory bank 410 includes a free list 502 that includes entries 504. In one exemplary embodiment, each entry 504 is 32 bits and is configured as a pointer to an address in memory bank 410” (par. 0040; fig. 5 and related text)**].

Goldberg (US 6,874,062), Lehman (US 6,658,437) and Rozario et al. (US 204/0078525) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit as taught by Goldberg to have the first state includes at least a portion of a memory address of an available first memory block as taught by Lehman, since Lehman discloses doing so would provide the benefit of creating [**“a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions” (Col. 2, lines 42-48)**]; and to further modify the combination of Goldberg and Lehman so that a logic circuit comprising a state indicating memory availability comprises at least a portion of a memory address, irrespective of a position of the logic circuit, in the manner taught by Rozario wherein a logic circuit indicating memory availability comprises memory addresses of free or available



Art Unit: 2185

memory blocks since doing so would allow the combined system of Goldberg and Lehman to **[provide higher speed and efficiency in memory accesses (Refer to Rozario, pars. 0005, 0051 and 0056)]**.

Therefore, it would have been obvious to combine Goldberg (US 6,874,062) with Lehman (US 6,658,437) and Rozario et al. (US 204/0078525) for the benefit of creating a memory management circuit to obtain the invention as specified in claim 1.

9. As per **claim 2**, the combination of Goldberg, Lehman and Rozario discloses the memory management circuit of claim 1, further comprising a second logic circuit associated with a first memory segment of the first memory block, the second logic circuit having a first state when the first memory segment is available for data storage and a second state when the first memory segment is not available for data storage **[Goldberg discloses “in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File” (Col. 8, lines 43-48) wherein “each of the bits in Bitmap 316 correspond to an associated one of Sections 0 through 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation” (Col. 7, lines 50-61) (Figure 3 and related text)]**.

10. As per **claim 3**, the combination of Goldberg, Lehman and Rozario discloses the memory management circuit of claim 1, wherein the second state is a state of a single logic bit **[Goldberg discloses “a bit is set if a Section is in use and is cleared if the Section is available for allocation” (Col. 7, lines 50-61). Lehman also discloses this limitation, as a bit is 1 to represent allocated memory (See Figure 9 and related text) which corresponds to a second state]**.

Art Unit: 2185

11. As per **claim 4**, the combination of Goldberg, Lehman and Rozario discloses The memory management circuit of claim 1 wherein the second state comprises information of an offset to a next available memory block or memory segment [**Goldberg discloses “by skipping portions of the LLB that are not associated with available memory, the search is completed more efficiently” (Col. 10, lines 25-29). Lehman discloses “pointer array 124 permit the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size” (Col. 9, lines 53-60) wherein “the pointer array 124 might point to a buddy segment that is available, but on other occasions the pointer array might point to a segment that was recently allocated. Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment” (Col. 10, lines 1-10) (Figure 7 and related text); therefore, a memory state indicating certain portions of memory are not available comprises information of the location or offset of free/available memory**].

12. As per **claim 5**, the combination of Goldberg, Lehman and Rozario discloses the memory management circuit of claim 1, further comprising a second logic circuit having a plurality of logic sub-circuits, each logic sub-circuit corresponding to a respective one of the memory segments of the first memory block, each logic sub-circuit having a first state when its respective memory segment is available for data storage and a second state when its respective memory segment is not available for data storage [**Goldberg discloses Lowest Level Bitmap (LLB) wherein “in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the**

Art Unit: 2185

**hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections (*interpreted to correspond to the claimed memory segments*). That is, the LLB contains a bit for each Section in a File” (Col. 8, lines 43-48) wherein “each of the bits in Bitmap 316 correspond to an associated one of Sections 0 through 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation” (Col. 7, lines 50-61) (Figure 3 and related text).].**

13. As per **claim 6**, the combination of Goldberg, Lehman and Rozario discloses The memory management circuit of claim 2, wherein the first state of the second logic circuit comprises at least a portion of a memory address of the first memory segment [**The rationale in the rejection to claim 1 is herein incorporate; further note at least a portion of a memory address of a memory also comprises at least a portion of the address of memory segments within the memory block**].

14. As per **claim 7**, the combination of Goldberg, Lehman and Rozario discloses the memory management circuit of claim 2, discloses a third logic circuit that converts the first state of the first logic circuit and the first state of the second logic circuit to the memory address of the first memory segment as [**Goldberg teaches performing a top-down search of hierarchical bitmap structures in which “if such a string is located, processing continues... If an address is returned indicating that the desired available memory had been located, each of the bits in the Current\_BML that corresponds to a bit described by Saved\_Bits must be set to an appropriate state... the state indicated whether or not the bit corresponds to memory that has been entirely allocated” (Col. 14, lines 38-57) (Figures 8A-9D and related text) wherein “the memory address associated with the located available memory sections may be**

Art Unit: 2185

returned to the requester" (col. 12, lines 26-29). Leham discloses "blocks larger than 1 can start only on an appropriate block address... the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array" (Col. 10, line 61-Col. 11, line 5) (Figure 9 and related text)].

15. As per **claim 8**, the combination of Goldberg, Lehman and Rozario discloses the memory management circuit of claim 2, wherein the first and second states of the first logic circuit are states of a plurality of logic bits and the first and second states of the second logic circuit are states of a plurality of digital bits [**Goldberg discloses first and second states of first and second logic circuits such as LLB and Bitmap 1, comprising a plurality of logic bits (fig. 6 and related text)**]. Lehman discloses "the second type of allocation bit map, where size=0, is used for blocks that are sixteen times the unit size, or larger... In the second type bit map, the first byte is the status byte for the buddy segment" (Col. 11, lines 47-57); therefore, having a plurality of bits representing states/status].

16. As per **claim 9**, the combination of of Goldberg, Lehman and Rozario discloses the memory management circuit of claim 2, wherein the first state of the second logic circuit is indicative of a memory offset between the memory address of the first memory block and the memory address of the first memory segment [**The rationale in the rejection to claim 4 is herein incorporated**].

Art Unit: 2185

17. As per **claim 24**, Goldberg discloses a method for managing memory, the method comprising: analyzing a state of a first logic circuit to determine whether a block of memory segments includes a memory segment that is available for data storage, the first logic circuit having a first state when the block of memory segments has a memory segment that is available for data storage and a second state when the block of memory segments does not have a memory segment that is available for data storage; **[Goldberg discloses this limitation as “an Operating System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System” (Col. 7, lines 11-13) wherein “in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections (*interpreted to correspond to the claimed memory segments*). That is, the LLB contains a bit for each Section in a File” (Col. 8, lines 43-48) and explains “the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB (*interpreted to correspond to the claimed blocks*). This bitmap, which may be referred to as Bitmap 1 (*interpreted to correspond to the claimed first logic circuit*), will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to “0” if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to “1” if all bits in the corresponding LLB Segment are set” (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein “a bit is set if a Section is in use and is cleared if the Section is available for allocation” (Col. 7, lines 50-61)]**

Art Unit: 2185

and if the block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the block of memory segments that is available for data storage [Goldberd discloses “...a bit in the first BML is cleared to indicate memory availability if any of the bits in the corresponding Segment of the LLB is cleared, indicating memory availability” (col. 4, lines 46-56) “a search for an available storage Segment of a predetermined length” (Col. 11, lines 23-28) (Figures 8A-9D and related text) wherein “the memory address associated with the located available memory sections may be returned to the requester” (col. 12, lines 27-29)].

Goldberg does not expressly disclose wherein the first state comprises at least a portion of a memory address of the block of memory segments irrespective of a position of the first logic circuit.

Lehman discloses having the first state includes at least a portion of a memory address of the first memory block as [“The DBMS 24 receives database requests from the clients 28 and performs data access operations to storage and retrieve referenced data values from the storage subsystem 30... the DBMS 24 maintains data structures called allocation pages that keep track of data storage availability” (Col. 3, line 61-Col. 4, line 37) having an allocation array wherein “blocks larger than 1 can start only on an appropriate block address... the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two” (Col. 11, lines 38-46) (Figure 7 and related text) and explains “the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array... For example, for size=1, the

Art Unit: 2185

**pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks” (Col. 10, line 50-Col. 11, line 15) (Figure 9 and related text) and explains “FIG. 9 shows an allocation array that includes 5 groups of bitmaps each having 16 bits... there are 16 bits in a group, each having 16 address locations numbered 0-15” (col. 10, lines 50-60)]; therefore, bits which represent a first state and indicate availability of a memory block correspond to bits having “a first state” wherein since the bit position of these bits has a memory address, thus, disclosing first state includes at least a portion of a memory address of the memory block having available memory, as claimed. Note that the bits representing a first state in Lehman have a direct correspondence with their calculated memory address, thereby, “*comprising*” at least a portion of their memory address].**

Rozario discloses a logic circuit/method having a state indicating availability of memory, wherein a state indicating memory availability comprises at least a portion of a memory address, irrespective of a position of the first logic circuit as [**“each memory bank 410 includes a free list 502 that includes entries 504. In one exemplary embodiment, each entry 504 is 32 bits and is configured as a pointer to an address in memory bank 410” (par. 0040; fig. 5 and related text)]].**

Goldberg (US 6,874,062), Lehman (US 6,658,437) and Rozario et al. (US 204/0078525) are analogous art because they are from the same field of endeavor of computer memory access and control.

Art Unit: 2185

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system/method as taught by Goldberg to have the first state includes at least a portion of a memory address of an available first memory block as taught by Lehman, since Lehman discloses doing so would provide the benefit of creating [**“a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions” (Col. 2, lines 42-48)**]; and to further modify the combination of Goldberg and Lehman so that a logic circuit comprising a state indicating memory availability comprises at least a portion of a memory address, irrespective of a position of the logic circuit, in the manner taught by Rozario wherein a logic circuit indicating memory availability comprises memory addresses of free or available memory blocks since doing so would allow the combined system of Goldberg and Lehman to [**provide higher speed and efficiency in memory accesses (Refer to Rozario, pars. 0005, 0051 and 0056)**].

Therefore, it would have been obvious to combine Goldberg (US 6,874,062) with Lehman (US 6,658,437) and Rozario et al. (US 204/0078525) for the benefit of creating a method to obtain the invention as specified in claim 24.

18. **Claims 10, 12-15 and 26-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldberg (US 6,874,062) in view of Lehman (US 6,658,437)

19. As per **claim 10**, Goldberg discloses a memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising: [**Goldberg discloses “an Operating**



Art Unit: 2185

**System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System” (Col. 7, lines 11-13) wherein “Files can further be subdivided into smaller addressable portions of memory called “sections,” (*interpreted to correspond to the claimed memory segments*) wherein each section has a same predetermined size” (Col. 7, lines 22-26) and explains grouping sections into segments (*interpreted to correspond to the claimed memory block*) (Col. 8, lines 49-65) (Figures 1 and 2 and related text)]**

a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage; [**Goldberg teaches Bitmap 1 wherein “in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File” (Col. 8, lines 43-48) and explains “the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to “0” if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to “1” if all bits in the corresponding LLB Segment are set” (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein “a bit is set if a Section is in use and is**

Art Unit: 2185

**cleared if the Section is available for allocation” (Col. 7, lines 50-61). See Bitmap arrangement in if fig. 6 and related text]**

a second logic circuit having a first state when a first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for data storage; and a third logic circuit having a first state when a second memory segment of the first memory block is available for data storage and a second state when the second memory segment of the first memory is not available for data storage;

**[Goldberg discloses Lowest Level Bitmap (LLB) wherein "in a hierarchical bitmap scheme..., the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 through 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text)]**

wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to at least the first state of the second logic circuit and the first state of the third logic circuit **[With respect to this limitation, Goldberg discloses “a bitmap structure is defined that allows N contiguous search items to be located wherein all search items in the set have a same predetermined attribute. The system and method may be adapted for use in locating N contiguous sections of memory all having the same predetermined attribute. Namely the contiguous sections are all available for allocation” (Col. 8, line 23-32) wherein figure 6 teaches each state of a higher level bitmap or bitmap 1 comprises an available number of**

Art Unit: 2185

**memory sections (or segments) in a lower level bitmap or LLB (fig. 6 and related text; col. 4, lines 4-56)],** however, Goldberg does not explicitly disclose the first logic circuit comprises a number of available memory segments

wherein the first state of the first logic circuit is separate from the first state of the second logic circuit and the first state of the third logic circuit [**the states of bitmap 1 are shown as being separate from the states representing sections of the LLB (fig. 6 and related text)]**].

Lehman discloses wherein a state of a logic circuit comprises a number of available memory segments in a first memory block, said number of available memory segments corresponding to the first state of the second logic circuit or to the state of a logic circuit indicating availability of memory segments as [**“for the first type of bit map, where the size bit is set to size=1, the bits are examined as individual bits, and logical groups inside the 16 bits must be determined by examining adjacent bits. For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks-they are never subdivided” (Col. 11, lines 6-14) and further discloses “as the buddy segments... are allocated... the count array 122 and the pointer array 124 are updated to indicate the current count of free blocks” (col. 10, lines 11-25; fig. 7 and related text)]**].

Goldberg (US 6,874,062) and Lehman (US 6,658,437) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit as taught by Goldberg and further explicitly

Art Unit: 2185

define that first state comprising a number of available memory segments in the first memory block as taught by Lehman.

The motivation for doing so would have been because Lehman discloses [**“a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions” (Col. 2, lines 42-48)**].

Therefore, it would have been obvious to combine Lehman (US 6,658,437) with Goldberg (US 6,874,062) for the benefit of creating a memory management circuit to obtain the invention as specified in claim 10.

20. As per **claim 12**, the combination of Goldberg and Lehman discloses The memory management circuit of claim 11, wherein the first and second states of the second and third logic circuit are single-bit logic states [**Goldberg discloses “a bit is set if a Section is in use and is cleared if the Section is available for allocation” (Col. 7, lines 50-61). Refer to Bitmap structures in fig. 6 and related text. Lehman also discloses this limitation, as a bit is 1 to represent allocated memory (See Figure 9 and related text) which corresponds to a second state**].

21. As per **claim 13**, Goldberg discloses a memory management system for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management system comprising: a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are

Art Unit: 2185

available for storage; [**“in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections (*interpreted to correspond to the claimed memory sections*). That is, the LLB contains a bit for each Section in a File” (Col. 8, lines 43-48) “a bitmap is then created to define the Segments (*interpreted to correspond to the claimed memory blocks*) of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to “0” if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to “1” if all bits in the corresponding LLB Segment are set” (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein “a bit is set if a Section is in use and is cleared if the Section is available for allocation” (Col. 7, lines 50-61)].**

wherein the second state of the first logic circuit comprise information indicating an offset to available memory [**Goldberg discloses “by skipping portions of the LLB that are not associated with available memory, the search is completed more efficiently” (Col. 10, lines 25-29)**] but doesn’t expressly disclose the second state of the first logic circuit comprise information indicating an offset to available memory.

Lehman discloses the second state of the first logic circuit comprises an offset to available memory as [**“pointer array 124 permits the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size” (Col. 9, lines 53-60)**

Art Unit: 2185

**wherein “the pointer array 124 might point to a buddy segment that is available, but on other occasions the pointer array might point to a segment that was recently allocated. Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment” (Col. 10, lines 1-10) (Figure 7 and related text)].**

Goldberg and Lehman are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit as taught by Goldberg and further specifically have the second state of the first logic circuit comprise information indicating an offset to available memory as taught by Lehman.

The motivation for doing so would have been because Lehman discloses [**“a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions” (Col. 2, lines 42-48)**].

Therefore, it would have been obvious to combine Lehman with Goldberg for the benefit of creating a memory management circuit to obtain the invention as specified in claim 13.

22. As per claim 14. (Previously Presented) The memory management circuit of claim 13, further comprising a second logic circuit having a first state when a first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for storage [**Goldberg teaches Lowest Level**

Art Unit: 2185

**Bitmap (LLB) wherein “each bit in the LLB corresponds to a section of storage. A bit may be set to a predetermined state, for example “0”, to indicate that the corresponding memory section is available for allocation. A first BLM is then defined to describe this LLB... a bit in the first BML is cleared to indicate memory availability if any of the bits in the corresponding Segment of the LLB is cleared, indicating memory availability” (col. 4, lines 46-56)].**

23. As per claim 15. (Previously Presented) The memory management system of claim 14, wherein the second state of the second logic circuit comprises an offset to an available memory segment [Lehman teaches “the pointer array 124 might point to a buddy segment that is available, but on other occasions the pointer array might point to a segment that was recently allocated. Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment” (Col. 10, lines 1-10) (Figure 7 and related text)].

24. As per claim 26. A method for managing memory, the method comprising:  
analyzing a state of a first logic circuit to determine whether a block of memory segments  
includes a memory segment that is available for data storage, the first logic circuit having a first  
state when the block of memory segments has a memory segment that is available for data  
storage and a second state when the block of memory segments does not have a memory segment  
that is available for data storage; and [Goldberg discloses this limitation as “an Operating System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System” (Col. 7, lines 11-13) wherein “in a hierarchical bitmap scheme... the

Art Unit: 2185

**Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections (*interpreted to correspond to the claimed memory segments*). That is, the LLB contains a bit for each Section in a File” (Col. 8, lines 43-48) and explains “the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB (*interpreted to correspond to the claimed blocks*). This bitmap, which may be referred to as Bitmap 1 (*interpreted to correspond to the claimed first logic circuit*), will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to “0” if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to “1” if all bits in the corresponding LLB Segment are set” (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein “a bit is set if a Section is in use and is cleared if the Section is available for allocation” (Col. 7, lines 50-61)]**

if the block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the block of memory segments that is available for data storage, [Goldberd discloses “...a bit in the first BML is cleared to indicate memory availability if any of the bits in the corresponding Segment of the LLB is cleared, indicating memory availability” (col. 4, lines 46-56) “a search for an available storage Segment of a predetermined length” (Col. 11, lines 23-28) (Figures 8A-9D and related text) wherein “the memory address associated with the located available memory sections may be returned to the requester” (col. 12, lines 27-29)] wherein: each of the memory segments is associated with



Art Unit: 2185

a respective second logic circuit having a first state when the memory segment of the block of memory segments is available for data storage and a second state when the memory segment of the block of memory segments is not available for data storage; and **[Goldberg discloses Lowest Level Bitmap (LLB) wherein "in a hierarchical bitmap scheme..., the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 through 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text)]**

the first state of the first logic circuit comprises a number of available memory segments in the block of memory segments, said number of available memory segments corresponding to the first state of each of the respective second logic circuits **[With respect to this limitation, Goldberg discloses "a bitmap structure is defined that allows N contiguous search items to be located wherein all search items in the set have a same predetermined attribute. The system and method may be adapted for use in locating N contiguous sections of memory all having the same predetermined attribute. Namely the contiguous sections are all available for allocation" (Col. 8, line 23-32) wherein figure 6 teaches each state of a higher level bitmap or bitmap 1 comprises an available number of memory sections (or segments) in a lower level bitmap or LLB (fig. 6 and related text; col. 4, lines 4-56)],** however, Goldberg does not explicitly disclose the first logic circuit comprises a number of available memory segments.

Art Unit: 2185

Lehman discloses wherein a state of a logic circuit comprises a number of available memory segments in a first memory block, said number of available memory segments corresponding to the first state of the second logic circuit or to the state of a logic circuit indicating availability of memory segments as [**“for the first type of bit map, where the size bit is set to size=1, the bits are examined as individual bits, and logical groups inside the 16 bits must be determined by examining adjacent bits. For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks-they are never subdivided”** (Col. 11, lines 6-14) and further discloses **“as the buddy segments... are allocated... the count array 122 and the pointer array 124 are updated to indicate the current count of free blocks”** (col. 10, lines 11-25; fig. 7 and related text)].

Goldberg (US 6,874,062) and Lehman (US 6,658,437) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit as taught by Goldberg and further explicitly define that first state comprising a number of available memory segments in the first memory block as taught by Lehman.

The motivation for doing so would have been because Lehman discloses [**“a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions”** (Col. 2, lines 42-48)].

Art Unit: 2185

Therefore, it would have been obvious to combine Lehman (US 6,658,437) with Goldberg (US 6,874,062) for the benefit of creating a memory management circuit to obtain the invention as specified in claim 26.

25. As per **claim 27**, the combination of Goldberg and Lehman discloses the second state of the first logic circuit comprises information indicating an offset to available memory as Lehman discloses [**“pointer array 124 permits the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size” (Col. 9, lines 53-60) wherein “the pointer array 124 might point to a buddy segment that is available, but on other occasions the pointer array might point to a segment that was recently allocated. Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment” (Col. 10, lines 1-10) (Figure 7 and related text); therefore, a memory state indicating certain portions of memory are not available comprises information indicating of the location or offset of free/available memory**].

#### **ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT**

##### **Response to Amendment**

26. Applicant's arguments filed on 3/5/2010 have been fully considered but are not deemed persuasive.

27. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

**ARGUMENTS CONCERNING PRIOR ART REJECTIONS**

28. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

29. Applicant argues that Applicant's Specification provides support for the limitations of “wherein the first state comprises at least a portion of a memory address of the first memory block, irrespective of a position of the first logic circuit” (claim 1) and “the first state comprises at least a portion of a memory address of the block of memory segments irrespective of a position of the first logic circuit” (claim 25) in the recitation that “The address-determining step 1040 may be accomplished in a variety of ways... various information may be contained in the segment or block flags... utilize to calculate the segment address. Alternatively, for example, the step 1040 may convert the position of the identified segment flag... to the address of the memory segment” (Specification, paragraph 96) and that these claim limitations are “clearly supported by Applicant’s explicit teachings of using information contained in the segment or block flags to calculate the segment address instead of (i.e., alternatively) converting the position of the identified segment flag and/or the identified block flag”.

In response, these arguments have been fully considered but are not deemed persuasive since the recitation in Applicant’s Specification does not specify anywhere what kind of information may be contained in the segment or block flags or whether addresses of segments or blocks are “irrespective of the position of the first logic circuit” or the logic circuit comprising information indicating memory availability. Further, Applicant's recitation does not specify how

Art Unit: 2185

the "various information" that may be contained in the segment or block flags is utilized to calculate the segment address, and the mere recitation that "The address-determining step 1040 may be accomplished in a variety of ways... various information may be contained in the segment or block flags... utilize to calculate the segment address. Alternatively, for example, the step 1040 may convert the position of the identified segment flag... to the address of the memory segment" (Specification, paragraph 96) does not imply that the various types of information is "irrespective of the position of the first logic circuit" since it simply lacks description of any alternative ways. However, all the described ways of calculating the address do show the address depending on the position of the logic circuits; **(refer to figs. 2-9 and related text)** which illustrate addresses of identified available memory blocks corresponding to the position of logic circuits 450.

30. In response to Applicant's argument that the combination of Goldberg and Lehman does not disclose "wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to the first state of the second logic circuit" and "wherein the first state of the first logic circuit is separate from the first state of the second logic circuit and the first state of the third logic circuit", that "Lehman's bit map corresponds to available memory segments, not first states of second and third logic circuits" and that Lehman fails to teach that the first state of the first logic circuit is separate from the first state of the second logic circuit and the first state of the third logic circuit.

In response, these arguments have been fully considered, but they are not deemed persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The combination of Goldberg and Lehman discloses “wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to the first state of the second logic circuit” and “wherein the first state of the first logic circuit is separate from the first state of the second logic circuit and the first state of the third logic circuit” as Goldberg discloses **[bitmap 1 (corresponding the claimed first logic circuit) wherein each state in bitmap 1 corresponds to a number of sections of memory pointed to by LLB (which comprises a second logic circuit comprising a first state and a separate and third logic circuit comprising a first state)** (See fig. 6 and related text of Goldberg), wherein Goldberg further discloses “a bitmap structure is defined that allows N contiguous search items to be located wherein all search items in the set have a same predetermined attribute. The system and method may be adapted for use in locating N contiguous sections of memory all having the same predetermined attribute. Namely the contiguous sections are all available for allocation” (Col. 8, line 23-32) wherein figure 6 teaches each state of a higher level bitmap comprises an available number of memory portions in a lower level bitmap (fig. 6 and related text; col. 4, lines 4-56). Applicant should note, that every bit of Bitmap 1 comprises a number of available memory

Art Unit: 2185

**sections/segments in LLB; wherein the Bitmap hierarchy depicted comprises more levels such as Bitmap 2 and Bitmap 3 (Fig. 6 and related text)];** however, Goldberg is not explicit in reciting the first state of bitmap 1 comprising a number of available memory segments.

Lehman explicitly discloses wherein a state of a logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to the first state of the second logic circuit or to the state of a logic circuit indicating availability of memory segments as [**“for the first type of bit map, where the size bit is set to size=1, the bits are examined as individual bits, and logical groups inside the 16 bits must be determined by examining adjacent bits. For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks-they are never subdivided” (Col. 11, lines 6-14) and further discloses “as the buddy segments... are allocated... the count array 122 and the pointer array 124 are updated to indicate the current count of free blocks” (col. 10, lines 11-25; fig. 7 and related text)]. Thus, clearly discloses bits indicating availability of memory comprise a number of available/free portions of memory. Therefore, in view of Lehman's disclosure, one of ordinary skill in the art would appreciate that each bit of bitmap 1 of Goldberg comprises a number of sections of memory pointed to by the LLB which comprises 1 bit to indicate availability or unavailability of memory sections.**

31. Regarding Applicant's remark that the combination of Goldberg and Lehman does not disclose “wherein the second state of the first logic circuit comprises information indicating an

Art Unit: 2185

offset to available memory” as “Lehman discloses... the pointer array actually provides a hint to the location of a free buddy segment... different than “wherein the second state of the first logic circuit comprises information indicating an offset to available memory.”

In response, these arguments have been fully considered, but they are not deemed persuasive.

The combination of Goldberg and Lehman discloses “wherein the second state of the first logic circuit comprises an offset to available memory” as Lehman discloses [**“pointer array 124 permit the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size” (Col. 9, lines 53-60) wherein “the pointer array 124 might point to a buddy segment that is available). Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment” (Col. 10, lines 1-10) (Figure 7 and related text)**]; *wherein Applicant should note that in case that the offset points to an available memory segment, the offset comprises “an offset to available memory” and in case that the memory segment has been allocated and the offset has not been allocated, then the offset comprises an offset to a location to start looking for available memory; thus, Lehman discloses the claimed limitation of an offset to available memory and more, since in the case that for some reason this memory is no longer available the offset still points to a place where to start looking for available memory, which comprises “an offset to available memory”. Further, the pending claims do not contain any requirement or limitation precluding*



Art Unit: 2185

*the offset as taught by the combination of Goldberg and Lehman from reading on the claimed "offset to available memory."*

Additionally, claim 27 requires information indicating an offset to available memory and the response presented on the non-final office action mailed on 11/5/2009 regarding claim 27 still applies to the rejection of claim 27.

32. Applicant argues there is motivation to combine Goldberg with Lehman and Rozario or combining Goldberg with Lehman, that the combination would be inoperable and that Goldberg teaches away from the solutions provided by Lehman; and that the motivation provided by the Examiner for combining Rozario is not proper since the motivation does not apply to the proposed modifications.

In response, these arguments have been fully considered but are not deemed persuasive.

In view of the following discussion, Examiner would like to emphasize the following:

Sources of rationale supporting a rejection under 35 U.S.C. 103 may be in a reference, or reasoned from common knowledge in the art, scientific principles, art recognized equivalents, or legal precedent. The CCPA has held that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom." In re Preda, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968); MPEP 2144.01.

In determining obviousness under 35 U.S.C. 103 in view of the Supreme Court decision in KSR International Co. v. Teleflex Inc., the Supreme Court stated that: "If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it

Art Unit: 2185

would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill”.

Still further, the Court states that “the focus when making a determination of obviousness should be on what a person of ordinary skill in the pertinent art would have known at the time of the invention...and this is regardless of whether the source of that knowledge and ability was documentary prior art, general knowledge in the art, or common sense”.

In response to Applicant’s remark that there is no motivation to combine Goldberg and Lehman and Rozario the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Goldberg and Lehman are involved and directed to memory access and control, more specifically, optimizing memory allocation by indicating available/unavailable memory wherein one of ordinary skill in the art would recognize that modifying Goldberg as taught by Lehman would provide the advantages of [**“a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions” (Col. 2, lines 42-48)**], as taught by Lehman. It would have further been obvious to modify the combination of Goldberg and Lehman so that a logic circuit comprising a state indicating memory availability comprises at least a portion of a memory address, irrespective of a position of the logic circuit, in the manner

Art Unit: 2185

taught by Rozario wherein a logic circuit indicating memory availability comprises memory addresses of free or available memory blocks since doing so would allow the combined system of Goldberg and Lehman to **[provide higher speed and efficiency in memory accesses (Refer to Rozario, pars. 0005, 0051 and 0056)]**; wherein Applicant should note that doing so would speed memory access since the circuit comprising information on availability of memory also comprises memory addresses of the available memory, which would simplify memory access calculations and provide fast and efficient access to memory.

33. In response to applicant's arguments regarding the incorporation of Lehman's and Rozario's teachings with the Goldberg reference, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

34. Regarding Applicant's remark that Goldberg teaches away from the combination with Lehman as Goldberg teaches away from using multiple bits representations since Goldberg touts the advantage of single bit representations; this argument has been fully considered but it is not deemed persuasive.

35. In response to applicant's argument that Goldberg teaches away from its combination with Lehman, the Examiner would like to point out that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the

Art Unit: 2185

references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

The Examiner would also like to point out that the reference to Goldberg does not teach away from the possibility of combining Goldberg with Lehman to obtain the claimed invention as Goldberg's disclosure does not criticize, discredit, or otherwise discourage the solution claimed *In re Fulton*, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004). See also MPEP 2123.

36. Regarding Applicant's remark that the cited portions of Lehman teach pointer arrays to search for free blocks, which would teach away from the claimed invention. This remark has been fully considered but it is not deemed persuasive as Lehman discloses [**"pointer array 124 permit the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size"** (Col. 9, lines 53-60) wherein **"the pointer array 124 might point to a buddy segment that is available, but on other occasions the pointer array might point to a segment that was recently allocated. Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment"** (Col. 10, lines 1-10) (Figure 7 and related text)]; therefore, a memory state indicating certain portions of memory are not available comprises information of the location of free/available memory; disclosing a second state which comprises information indicating an offset to available memory.

Art Unit: 2185

37. In view of the foregoing, the Examiner would like to emphasize the combinations of Goldberg and Lehman; and Goldberg Lehman and Rozario are deemed proper and disclose the limitations required by the claims.

38. All arguments by the applicant are believed to be covered in the body of the office action; thus, this action constitutes a complete response to the issues raised in the remarks dated 3/5/2010.

### **CONCLUSION**

39. Any new of rejection presented in this Office action were necessitated by Applicant's amendments filed on 3/5/2010. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

#### **a. STATUS OF CLAIMS IN THE APPLICATION**

Art Unit: 2185

40. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

**a(1) CLAIMS REJECTED IN THE APPLICATION**

41. Per the instant office action, claims 1-10, 12-15, 24 and 26-27 have received an on the merits and are subject of a final rejection.

**a(2) CLAIMS REJECTED IN THE APPLICATION**

42. Claims 11, 16-23, 25 and 28-40 have been canceled as of Applicant's submission filed on 3/5/2010.

**b. DIRECTION OF FUTURE CORRESPONDENCES**

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232, and email address is [yaima.campos@uspto.gov](mailto:yaima.campos@uspto.gov). The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

44. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions

Art Unit: 2185

on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 4, 2010

/Yaima Campos/  
Examiner, Art Unit 2185

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185